Applicati n N .: 09/801,350 **Docket No.: JCLA6643-R2**

AMENDMENTS

In The Claims:

Please amend the claims by amending claims 1 and 3, and canceling claim 14, according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

1. (currently amended) An electrostatic discharge (ESD) protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising:

a silicon controlled rectifier (SCR) circuit, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage, so as to discharge the electrostatic charges; and

an anti-latch-up circuit, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage, and the third connection terminal of the SCR circuit, wherein the sixth connection terminal of the anti-latch-up circuit is directly connected to the third connection terminal of the SCR circuit, whereby an anti-latch-up signal is sent from the sixth connection terminal to the SCR circuit during normal operation.

2. (original) The ESD protection circuit of claim 1, further comprising:

a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and

a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

3. (currently amended) The ESD protection circuit of claim 1, wherein the SCR circuit comprises:

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a P-type substrate;

an N well, formed in the p-type substrate;

a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage;

a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage;

a second N+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, ~~and~~ coupled via the third connection terminal of SCR circuit to the sixth connection terminal of the anti-latch-up circuit, serving as a guard ring to collect electrons to avoid latch up when the anti-latch-up circuit sends the anti-latch-up signal through the sixth connection terminal to the third connection terminal of the SCR circuit during normal operation, and floating when the anti-latch-up circuit sends no signal to the SCR circuit during an ESD event;

a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/O pad; and

a third N+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source.

4. (original) The ESD protection circuit of claim 3, wherein the anti-latch-up circuit comprises:

a capacitor, having a first contact end and a second contact end, respectively coupled to the second N+ doped region and the ground voltage; and

a resistor, having a first end and a second end, respectively coupled to the voltage source and the second N+ doped region.

5. (withdrawn) The ESD protection circuit of claim 3, wherein the anti-latch-up circuit comprises:

a PMOS transistor, having a gate electrode, a source region coupled to the voltage source, and a drain region coupled to the second N+ doped region;

a resistor, having a first end and a second end, respectively coupled to the gate electrode of the PMOS transistor and the ground voltage; and

a capacitor, having a first contact end and a second contact end, respectively coupled to the voltage source and the gate electrode of the PMOS transistor.

6. (withdrawn) The ESD protection circuit of claim 1, wherein the SCR circuit comprises a low-voltage triggering SCR (LVTSCR) circuit, which comprises:

a P-type substrate;

an N well, formed in the p-type substrate;

a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage;

a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage;

a second N+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled to the sixth connection terminal of the anti-latch-up circuit, wherein an additional NMOS transistor with a source/drain region and a gate is formed between the first N+ doped region and the second N+ doped region;

a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/O pad; and

a third N+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source.

7. (withdrawn) The ESD protection circuit of claim 6, wherein the anti-latch-up circuit comprises:

a PMOS transistor, having a gate electrode, a source region coupled to the voltage source, and a drain region coupled to the second N+ doped region;

a resistor, having a first end and a second end, respectively coupled to the gate electrode of the PMOS transistor and the ground voltage; and

a capacitor, having a first contact end and a second contact end, respectively coupled to the voltage source and the gate electrode of the PMOS transistor,

wherein the gate electrode of the additional NMOS transistor of the LVTSCR circuit is also coupled to the gate electrode of the PMOS transistor.

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8. (withdrawn) The ESD protection circuit of claim 1, wherein the SCR circuit comprises:

a P-type substrate;

an N well, formed in the p-type substrate;

a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage;

a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage;

a second P+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled to the sixth connection terminal of the anti-latch-up circuit;

a third P+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the I/O pad; and

a second N+ doped region, formed in the N well, adjacent to the third P+ doped region, and coupled to the I/O pad.

9. (withdrawn) The ESD protection circuit of claim 8, wherein the anti-latch-up circuit comprises:

a capacitor, having a first contact end and a second contact end, respectively coupled to the voltage source and the second P+ doped region; and

a resistor, having a first end and a second end, respectively coupled to the second P+ doped region and the ground voltage.

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10. (withdrawn) The ESD protection circuit of claim 8, wherein the anti-latch-up circuit comprises:

an NMOS transistor, having a gate electrode, a source region coupled to the ground voltage, and a drain region coupled to the second P+ doped region;

a capacitor, having a first contact end and a second contact end, respectively coupled to the gate electrode of the PMOS transistor and the ground voltage; and

a resistor, having a first end and a second end, respectively coupled to the voltage source and the gate electrode of the PMOS transistor.

11. (withdrawn) The ESD protection circuit of claim 1, wherein the SCR circuit comprises a p-type low-voltage triggering SCR (LVTSCR) circuit, which comprises:

a P-type substrate;

an N well, formed in the p-type substrate;

a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage;

a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage;

a second P+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled to the sixth connection terminal of the anti-latch-up circuit;

a third P+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the I/O pad, wherein an additional PMOS transistor with a source/drain region and a gate electrode of the p-type LVTSCR circuit is formed between the second P+ doped region and the third P+ doped region; and

a second N+ doped region, formed in the N well, adjacent to the third P+ doped region, and coupled to the I/O pad.

12. (withdrawn) The ESD protection circuit of claim 11, wherein the anti-latch-up circuit comprises:

an NMOS transistor, having a gate electrode, a source region coupled to the ground voltage, and a drain region coupled to the second P+ doped region;

a capacitor, having a first contact end and a second contact end, respectively coupled to the gate electrode of the NMOS transistor and the ground voltage; and

a resistor, having a first end and a second end, respectively coupled to the voltage source and the gate electrode of the NMOS transistor,

wherein the gate electrode of the additional PMOS transistor of the p-type LVTSCR circuit is also coupled to the gate electrode of the NMOS transistor.

13. (previously added) The ESD protection circuit of claim 1, wherein the anti-latch-up signal sent from the sixth connection terminal to the SCR circuit comprises a voltage signal.

Claim 14. (currently canceled).